ABSTRACT

A system is disclosed in which an on-chip logic analyzer (OCLA) is included in an integrated circuit, such as a microprocessor. During debug modes, one or more sets of an on-chip cache memory are disabled from use by other circuitry in the integrated circuit, and reserved exclusively for use by the OCLA. Data stored in the reserved cache set can then be read out by the OCLA, and placed in a register that can be accessed by other logic internal or external to the integrated circuit. If the integrated circuit is operating under normal mode, the cache memory set can be used in conventional fashion by other circuitry with in the integrated circuit to enhance performance.